CLAIMS:

1. An automated test equipment – ATE - (200) having a tester-per-pin architecture with a plurality of individual decentralized per-pin testing units (700), each per-pin testing unit (700i) being adapted for testing a respective DUT-pin (di) of a device under test – DUT - (600) by emitting stimulus response signals to the respective DUT-pin and/or receiving stimulus response signals from the respective DUT-pin, wherein - during a testing sequence - the DUT (600) is defined into one or more DUT-cores representing one or more functional units of the DUT (600) and covering one or more DUT-pins of the DUT (600); further comprising:

   means for assigning - during the testing sequence - one or more of the per-pin testing units (700i) to one or more ATE-ports (210-240), whereby each ATE-port comprises one or more of the per-pin testing units (700i) and represents an independent functional testing unit for testing one or more of the DUT-cores during the testing sequence.

2. The automated test equipment (200) of claim 1, wherein the means for assigning comprises:

   switching means for switching connections between one or more of the per-pin testing units (700i) and one or more of the DUT-pins, and

   controlling means for controlling the switching of the switching means in accordance with the assigning of the one or more of the per-pin testing units (700i) to the one or more ATE-ports (210-240) during the testing sequence.

3. The automated test equipment (200) of claim 1, wherein one of the ATE-ports (210-240) comprises programming means for independently

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defining and/or programming timing and/or stimulus/response pattern, as if the set of DUT-pins assigned to the one ATE-port constituted a device in itself.

4. The automated test equipment (200) of claim 3, wherein the programming means comprises:

means for specifying cycle times of stimulus and response vectors for the one ATE-port; and/or

means for specifying a per-pin timing in terms of sets of available waveforms for each ATE-pin of the one ATE-port, whereby each waveform represents a sequence of events of various types occurring at specified instances in time; and/or

means for specifying a pattern program for the one ATE-port; and/or

means for specifying a per-pin vector data for each pin of the one ATE-port; and/or

means for specifying analogue set-up conditions for analogue pins of the one ATE-port.

5. The automated test equipment (200) of claim 3 or 4, wherein the programming means comprises:

main pattern programs for implementing access protocols to one or more of the DUT-cores through a shared set of per-pin testing units (700i) constituting one individual ATE-port comprising at least the per-pin testing units (700i) that are part of the ATE-ports utilized to access the said one or more of the DUT-cores, and

independent pattern programs for implementing stimulus and response

patterns for each DUT-core of the said one or more of the DUT-cores.

6. The automated test equipment (200) of claim 5, wherein the main pattern program comprises:

means for configuring the one individual ATE-port for activating the per-pin testing units (700i) thereof for accessing the one or more of the DUT-cores to be accessed; and/or

means for selecting pattern data generated by the pattern programs of the accessed one or more of the DUT-cores during one testing sequence for testing the one or more of the DUT-cores to be accessed.

7. The automated test equipment (200) of claim 3, wherein the programming means comprises:

specifying means for specifying an alias mapping between per-pin testing units (700i) for a plurality of the ATE-ports, preferably for specifying timing information, a pattern program, or other test condition sets of one individual ATE-port to apply for the plurality of the ATE-ports for which the alias mapping is defined.

8. The automated test equipment (200) according to claim 1, further comprising specifying means for specifying overall test conditions for a test that concurrently operates on multiple ATE-ports.

9. The automated test equipment (200) of claim 8, wherein the specifying means comprises:

means for determining a set of concurrently active ATE-ports during a defined testing sequence; and/or

means for selecting the ATE-port test conditions for one or more ATE-

pins, preferably for selecting an ATE-port timing setup for one or more ATE-pins; and/or

means for specifying global test conditions to express dependencies between pins of the DUT and the ATE, preferably global DUT specifications; and/or

means for determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port.

10. A method for testing a device under test – DUT - (600) with an automated test equipment – ATE - (200) having a tester-per-pin architecture with a plurality of individual decentralized per-pin testing units (700), each per-pin testing unit (700i) being adapted for testing a respective DUT-pin (di) of the DUT (600) by emitting stimulus response signals to the respective DUT-pin and/or receiving stimulus response signals from the respective DUT-pin, the method comprising the steps of:

(a) defining – for a testing sequence - the DUT (600) into one or more DUT-cores representing one or more functional units of the DUT (600) and covering one or more DUT-pins of the DUT (600), and

(b) assigning - during the testing sequence - one or more of the per-pin testing units (700i) to one or more ATE-ports (210-240), whereby each ATE-port comprises one or more of the per-pin testing units (700i) and represents an independent functional testing unit for testing one or more of the DUT-cores during the testing sequence.

11. The method of claim 10, further comprising the step of:

(c) defining and/or programming timing and/or stimulus/response pattern for one or more of the ATE-ports (210-240), as if the set of

DUT-pins assigned to one of the ATE-ports constituted a device in itself.

12. The method of claim 11, wherein step (c) comprises one or more of the steps:

(c1) specifying cycle times of stimulus and response vectors for the one ATE-port;

(c2) specifying a per-pin timing in terms of sets of available waveforms for each per-pin testing unit (700i)of the one ATE-port, whereby each waveform represents a sequence of events of various types occurring at specified instances in time;

(c3) specifying a pattern program for the one ATE-port, preferably specifying common sequencing instructions for all per-pin testing units (700i) of the one ATE-port;

(c4) specifying per-pin vector data for each per-pin testing unit (700i) of the one ATE-port;

(c5) means for specifying analogue set-up conditions for analogue pins of the one ATE-port.

13. The method according to any one of the claims 9, further comprising a step of:

(d) specifying overall test conditions for a test that concurrently operates on multiple ATE-ports.

14. The method of claim 13, wherein step (d) comprises one or more of the steps:

(d1) determining a set of concurrently active ATE-ports during a defined testing sequence;

(d2) selecting the ATE-port test conditions for one or more ATE-pins, preferably for selecting an ATE-port timing setup for one or more ATE-pins;

(d3) specifying global test conditions to express dependencies between pins of the DUT and the ATE, preferably global DUT specifications;

(d4) determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port.

15. A software program or product, preferably stored on a data carrier, for executing the method according to claim 10, when run on a data processing system such as a computer.